IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	**09/807,686**
Appellant	:	**LEYDIER, Robert**
Filing Date	:	**04/30/2002**
Confirmation No	:	**2354**
Art Unit	:	**2892**
Examiner	:	**ARORA, Ajay**
Docket No.	:	**76.0531**
Customer No.	:	**41754**

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF (Revised)

1. Real Party in Interest

The real party in interest in this appeal is Gemalto N.V., a corporation of the Netherlands. The application is formally assigned to Axalto SA. Axalto, SA. is the French subsidiary of Gemalto.

2. Related Appeals and Interferences

There are no related appeals and interferences.

3. Status of Claims

Claims 1, 5-7, 10, 12-17 and 19-32 are pending in the application. Claims 2 and 3 have been withdrawn from consideration. Claims 4. 8, 9, 11 and 18 have been previously

cancelled. Claims 1,5-7, 10, 12-17 and 19-32 stand rejected in the Office Action of October 17, 2008. The rejections to Claims 1,5-7, 10, 12-17 and 19-32 are appealed herein.

4. Status of Amendments

An amendment to more clearly and distinctly claim the invention recited in Claim 21 is co-filed herewith for the purposes of eliminating the 35 USC 112, second paragraph rejection and consequently narrowing the issues for appeal. The claims listing of the Claims Appendix reflects the amendment made in the co-filed amendment.

5. Summary of Claimed Subject Matter

Claim 1 (directed, for example, to the embodiment illustrated in Figures 4a and 4c) is directed to a chip (5a) for a chip-containing portable article (1) comprising a silicon substrate layer (12a) having an active face (13a) with circuits integrated therein defining a central processor unit and memories; and an additional layer of silicon (14) that: is sealed to the active face of the silicon substrate layer by a sealing layer (15); covers at least part of said active face (Specification, Page 6, Line 17); and comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm (Page 6, Line 22 – Page 7, Line 7). As such the chip of Claim 1 addresses the problem of light based attacks used to switch transistors of the chip by exposing the chip to light in the IR spectrum.

Claim 20 is directed to a portable article provided with a chip a chip (5a, illustrated, for example, in Figures 4a and 4c) for a chip-containing portable article (1)

comprising a silicon substrate layer (12a) having an active face (13a) with circuits integrated therein defining a central processor unit and memories; and an additional layer of silicon (14) that: is sealed to the active face of the silicon substrate layer by a sealing layer (15); covers at least part of said active face (Specification, Page 6, Line 17); and comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm (Page 6, Line 22 – Page 7, Line 7). As such the chip of Claim 20 addresses the problem of light based attacks used to switch transistors of the chip by exposing the chip to light in the IR spectrum.

Claim 26 (directed, for example, to the embodiment illustrated in Figure 4b) is directed to a chip (5) for a chip-containing portable article having a silicon substrate layer (12) having an active face (13) with circuits integrated therein defining a central processor unit and memories; and physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm (Page 6, Line 22 – Page 7, Line 7) comprising silicon dopants in the face of the silicon substrate layer (12) that is opposite to the active face (Page 8, Lines 18-22, which describes that the dopants are located in the rear portion of the layer 12).

Claim 29 (directed, for example, to the embodiment illustrated in Figures 6a through 6d; Specification, Page 9, Line 3 – Page 10, Line7) is directed to a chip (Figure 2:5; Specification, Page 5, Lines 18 – 20; Figure 3a:5; Specification, Page Line 4; Figure 3B: 5a; Specification, Page 6, Line 8; Specification, Page 9, Lines 5 – 7; Page 9, Line 20 - 22) for a chip-containing portable article (Figure 1: 1; Page 5, Lines 12 - 17) having a

silicon substrate layer (Figure 3A: 12; Specification, Page 6, Line 4; Figure 3B: 12A; Specification, Page 6, Lines 8 – 11; Figure 6: 12, 12a) having an active face (Figure 3A: 13; Specification, Page 6, Lines 11 – 13) with circuits integrated therein defining a central processor unit and memories; and physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising surface irregularities (Figures 6A through D: 20; Specification, Page 9, Line 3 through Page 10, Line 7) in the face (6,6a) of the silicon substrate layer (12, 12a) that is opposite to the active face (Specification, Page 9, Lines 5 - 6).

Claim 30 (directed, for example, to the embodiment illustrated in Figure 7b, Specification, Page 10, Line 8 through Page 11, Line 5) is directed to a chip (Figure 2:5; Specification, Page 5, Lines 18 – 20; Figure 3a: 5; Specification, Page Line 4; Figure 7B: 5; Specification Page 10, Lines 21-22) for a chip-containing portable article (Figure 1: 1; Page 5, Lines 12 - 17) comprising a silicon substrate layer (Figure 3A: 12; Specification, Page 6, Line 4; Figure 3B: 12A; Specification, Page 6, Lines 8 – 11; Figures 7B: 12) having an active face with circuits integrated therein defining a central processor unit and memories; and physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising deposition of metal (Figure 7B: 21; Specification, Page 10, Lines 21 - 22, Line 5) on the face of the silicon substrate layer (12, 12a) that is opposite to the active face (Page 10, Lines 21-22).

6. Grounds for Rejection to be Reviewed on Appeal

35 USC 103(e)

Claims 1, 5-7, 14-17 and 19-23, 25-28 and 30-32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Orcutt (US 4,712,129, hereinafter "Orcutt") in view of Zhang (US 5,886,364, hereinafter "Zhang"). Claims 10, 12 and 13, 24 and 29 stand rejected under 35 USC 103(a) as being unpatentable over Orcutt, in view of Zhang and further in view of Kobachi, et al., (US 5,811,797, hereinafter "Kobachi").

7. Argument

The Examiner argues in the Office Action, that:

> Orcutt (refer to Figure 1) teaches a chip (12) that is capable of functioning as a chip-containing portable article, the chip comprising a silicon (Col. 1, lines 50-52) substrate layer (substrate layer of chip 12) having an active face with circuits integrated therein (Col. 2, lines 30-33), and an additional layer (18) of silicon (Col. 3, lines 3-5 and 41-42) that is sealed to the active face of the silicon substrate layer by a sealing layer (20), the additional layer of silicon (18) covering at least part of said active face (Col. 2, lines 30-33), the additional layer of silicon comprising physical means for providing physical protection (col. 3, lines 1-3). (Office Action, page 4, lines 9-16).

Further, the Examiner argues that the "[i]ntegraed circuits defining memories and associated central processor units are well known in the art" (Office Action, page 5, lines 1-2). The Examiner acknowledges that "Orcutt does not teach … b) that said additional layer of silicon comprises physical means for protection is such that the physical protection is 'against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1μm.'" Next, the Examiner argues that "Zhang teaches a semiconductor structure comprising a layer of silicon having a phosphorus dopant

concentration of about 10^{20} atoms per cm^3 (Col. 3, lines 31-34), which according to applicant's specification (see page 6, lines 5-24), provides physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1μm" (Office Action, page 5, lines 8-12). Finally, the Examiner argues:

> [i]t would have been obvious to one of ordinary skills in the art at the time of the invention to modify Orcutt such that the additional layer is a layer of silicon with the above described dopant concentration and thus comprises physical means for protection is such that the physical protection is against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm. The ordinary artisan would have been motivated to modify Orcutt for at least the purpose of providing protection to certain portions of the chip from incident light of the specific wavelengths that the device is expected to be exposed to. (Office Action, page 5, lines 12-19).

Turning now to the application of the principles of law to the present case. The first factor set forth in *Graham* is the ascertainment of the scope and content of the prior art. Consider first the Orcutt reference. Orcutt addresses two problems encountered in semiconductor IC devices: (1) the thermal expansion stress from large semiconductor bars exerted on the bar by the packaging (Orcutt, Col. 1, Lines 13-24) and (2) the detrimental effects of alpha particles penetrating to a memory device (Orcutt, Col. 1, Lines 25-39). Considering the reference to memory devices, one is lead to the inference that Orcutt deals with devices having a relatively large scale integration, e.g., LSI or VLSI devices.

The first of these problems is caused by encountering different thermal expansion rates in the plastic encapsulation, the semiconductor bar, and the bar pad. This causes a shear force, which may cause damage to the device.

The second problem had been solved before Orcutt by an alpha shield, e.g., a polymide tape. However, those solutions were deemed inadequate because moisture absorption.

To remedy these problems, Orcutt proposed a structure having a semiconductor bar 12 with active devices formed on the upper surface thereof and affixed to a bar pad 14 (illustrated in Figure 1 and described from Col. 2, Lines 17-43). A rigid planar member 18 is affixed to upper surface of the bar 12 with an adhesive film 20. According to Orcutt the planar member 18 may be approximately the same thickness of the bar, i.e., on the order of 10 mils (Col. 2, Lines 36-38). For purposes, of comparison made herein below it should be noted that 10mils is approximately 0.254 millimeters.

The upper surface of the planar member is grooved or otherwise textured to provide for mechanically locking the upper surface of the bar 12 to the encapsulating medium.

To summarize, Orcutt deals with thermal stresses between a semiconductor bar having thereon large scale integrated circuits such as memory devices by providing a relatively thick layer of silicon adhered thereto and which is textured to provide a locking mechanism to a plastic encapsulating medium.

Zhang deals with the problem of isolating individual transistors in a thin film transistor (TFT) device from incident light projected from behind the substrate of a TFT device to reduce the Ioff current of the TFT (Zhang, Col. 1, Lines 39-43).

One type of TFT device is liquid crystal display devices. TFTs are used to control the pixels in such devices. There is one TFT per pixel and that TFT is used to turn on-or-

off the pixel. Figure 4 of Zhang illustrates the operation of a TFT device. A light source is illuminated onto the device. TFT's 52 controlled via leads 53. The light is modified by a liquid crystal layer 60 and the modified light is seen from the side opposite the substrate. Zhang, Col. 6, Lines 34 – 62.

Since light must be transmitted through the pixel portions of the TFT device, it is ironic that light actually causes a problem with the TFTs, namely, the electronic conductivity of the active layer of a TFT increases as light is irradiated thereto. The increase in conductivity of an active layer unfavorably impairs the charge retention of a pixel electrode because the off current is increased by the irradiation of light. Zhang, Col. 1, Lines 23 – 32.

Zhang proposes a solution that includes a masking amorphous silicon film doped with phosphorous to act as a light shield to shut off the light irradiated from the substrate side. Zhang, Col. 2, Lines 36 – 59. The amorphous film of a thickness of 200-500 Angstrom (2.0×10^{-5} mm to 5.0×10^{-5} mm) is formed on a glass substrate. Zhang, Col. 3, Lines 28-30. Zhang states that the silicon film absorbs light and functions mainly as a light shield, Zhang, Col. 3, Lines 31-32, the with phosphorous doping is electrically conductive and maintains the potential to ground, Col. 3, Lines 34-37.

The amorphous silicon film is nitirided or oxidized in part to impart light transmitting properties thereto. The active region of a TFT is surrounded by a nitrided or oxidized portion whereas a light shielding layer extends under the active region to shield the TFT from light. Zhang, Col. 2, Lines 41-48.

To summarize, Zhang deals with masking light from individual transistors formed on a glass substrate of a TFT device thereby protecting the transistor from exposure to incident light which may cause the off current to increase.

Turning now to the second Graham factor, namely, the differences between the prior art and the claims at issue. Appellants address a problem of attacks using infrared light to obtain access to secrets stored in an IC chip. Appellants observe that attackers have sought to alter the processing of a chip by causing transistors in particular zones to switch by using focused electromagnetic radiation. This then causes the chip to perform operations that are normally not authorized, thus, giving access to secrets. Specification, Page 2, Lines 11 – 17. To avoid the vulnerability against light attacks, Appellants propose adding a layer of doped silicon to the integrated circuit device. For example, Figure 4A illustrates an additional layer of silicon with dopants, in Figure 4B, an alternative embodiment in which the silicon substrate layer have dopants in a rear portion thereof, and in Figure 4C dopants are present in both the additional layer an in the rear portion of the substrate layer. The dopants provide a physical means by which provide light absorption thereby protecting against light attacks.

The intrinsic silicon crystal is particularly vulnerable to penetration of infrared radiation. Specification, Page 7, Lines 8-14. Doping the silicon has been found to change the light absorption properties significantly at light wavelengths longer than 1 μm.

To summarize, Appellants provide an integrated circuit device in which an additional layer of doped silicon is added or doping is provided to a region of a silicon

substrate opposite the active region thereof. The layer of doped silicon provides a shielding against light used to perpetrate light attacks used to discern some information contained in the device.

Accordingly, Appellants claim "an additional layer of silicon that: is sealed to the active face of the silicon substrate layer by a sealing layer; covers at least part of said active face; and comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm." (Claim 1).

Neither Orcutt, nor Zhang, either alone or in combination teach or suggest an additional layer of silicon that comprises "physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm." The Examiner admits that "Orcutt does not teach that…said additional layer of silicon that comprises physical means for protection is such that the physical protection is 'against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm'." (Office Action, page 4, lines 17-21).

The Office Action relies on Zhang for teaching the doping of a silicon layer with phosphorus to a concentration of about 10^{20} atoms per cm^3 (Office Action, page 5, lines 8-9). Zhang fails to teach or suggest that phosphorus as a dopant in silicon "provides protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm."

Appellants respectfully submit that this is an incorrect reading of Zhang and application thereof to Orcutt.

Zhang teaches a thin film transistor that makes up a pixel element in a liquid crystal display, and a process for fabricating the same (Zhang, col. 1, lines 10-22). As an example, Zhang teaches "an amorphous silicon film 12 doped with phosphorous is formed at a thickness of 200-500 Å on a glass substrate 11. The silicon film absorbs light and function mainly as a light shield. The concentration of phosphorous contained in the amorphous silicon is $1x10^{19}$ atoms/cm^3 – $5x10^{21}$ atoms/cm^3, preferably $1\text{-}5x10^{20}$ atoms/cm^3" (Zhang, col. 3, lines 28-34). In Zhang, phosphorous doped silicon acts as a "light shield", but nowhere does Zhang specify the wavelength of light that is shielded. However, Zhang is directed to the creation of "electro-optical display device[s]" (col. 1, line58). As such, the light emitted onto the thin film transistors in the liquid crystal display can safely be assumed to be visible light (else the "display" function would be of no use). In this regard, the "light shield" is put in place because "the electric conductivity of the active layer of a TFT increases as light is irradiated thereto, because the active layers are made of a film of amorphous silicon or crystalline silicon which is usually photosensitive" (Zhang, col. 1, lines 25-28). There is, therefore, no reasonable way of interpreting the "light shielding" properties in Zhang to mean "radiation in the infrared range at a wavelength longer than 1 μm". As further proof, it is notable that the Office Action relies on Appellant's specification for teaching that "a layer of silicon having a phosphorus dopant concentration of about 10^{20} atoms per cm^3…provides protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm" (Office Action, page 5, lines 8-12). Therefore, neither Orcutt, nor Zhang, either alone or in combination teach or suggest an additional layer of silicon that comprises "physical means for providing physical protection against the action of

electromagnetic radiation in the infrared range at a wavelength longer than 1 μm", and Claim 1 is not obvious over Orcutt in view of Zhang.

Further, given the disclosure of Orcutt, Zhang teaches away from Claim 1. Zhang teaches a "an amorphous silicon film 12 doped with phosphorous … formed at a thickness of 200-500 Å on a glass substrate 11" where "[t]he silicon film absorbs light and function[s] mainly as a light shield" (col. 3, lines 28-32). However, such shielding action is performed well within the completed structure of the thin film transistor, as shown in Figures 1A-1G. This is because the phosphorous doped silicon layer is intended to shield the thin film transistor from light emitted from adjacent thin film transistors (Zhang, col. 1, lines 23-36). On the other hand, Claim 1 requires "a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and an additional layer of silicon that is sealed to the active face of the silicon substrate layer by a sealing layer", where the additional layer has "physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm". As such, Zhang's teaching of phosphorous doped silicon would need to be applied in the formation of the "silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories" (i.e., as part of the active structures of the central processor and memories). Therefore, Zhang teaches away from Claim 1, and Claim 1 is not obvious over Orcutt in light of Zhang.

Turning now to the appropriateness of combining Orcutt with Zhang. Orcutt and Zhang are from such disparate technology arts and for such different applications that the combination of Orcutt and Zhang could only be conceived in hindsight. Orcutt relates to semiconductor packaging considerations and shielding against alpha particles, and hence consists of structures and processes that take place after the circuit features making up the "integrated circuit" have been processed into the "bar" or substrate (col. 1, lines 13-39). On the other hand, Zhang relates to the creation of thin film transistors on a glass substrate for the making of a liquid crystal display. There are enormous differences between these disparate technologies, e.g., size, manufacturing technique, structure, purpose.

First, consider size. Appellants posit that the reader of this document is probably using a liquid crystal display such as a flat panel display monitor. The undersigned is writing these words using such a device. In the case of the undersigned, he is using a 23" diagonal monitor with a resolution of 1920 x 1200 pixels with physical dimensions of approximately 500mm x 300 mm. That results in a display having approximately 4 pixels or 4 transistors per mm. This may be considered fairly typical. Each pixel is controlled by one TFT. In contrast, Orcutt deals with integrated circuits. A contemporary integrated circuit was the Intel 80386 microprocessor. It contained 275,000 transistors. (Intel Museum – Microprocessor Hall of Fame, http://www.intel.com/museum/online/hist%5Fmicro/hof/, retrieved and printed on May 20, 2009) on a 100 square mm die (Intel 80386/80387 Memorabilia, CPU World, http://www.cpu-world.com/Memorabilia/80386/, retrieved and printed on May 20, 2009).

Thus approximately 2,750 transistors per mm. Thus, Orcutt deals with devices with three orders of magnitude higher density.

Orcutt's additional layer is approximately 10 mils or approximately 0.254 millimeters thick. In contrast, Zhang proposes a film that is a mere a thickness of 200-500 Angstrom (2.0×10^{-5} mm to 5.0×10^{-5} mm) thick. Even the larger of these 5.0×10^{-5} mm 5000 times thinner than Orcutt's 0.254 millimeter thick layer.

Manufacturing technique. As noted above in the discussion of Zhang, TFT devices are constructed on a glass substrate. Zhang, Col. 3, Lines 28-30. The layers of silicon are deposited thereon, for example, using plasma CVD or sputtering. Zhang, Col. 3, Lines 38-40. As noted above, the additional layer in Orcutt is approximately 0.254 mm thick. Appellants posit that the manufacturing techniques for producing such a layer is much different than the plasma CVD or sputtering techniques used in Zhang.

Structure. Orcutt describes an integrated circuit device formed using an integrated circuit bar that is about 10 mils thick. This bar, the bar pad, and the additional rigid planar member are encased in an encapsulating medium, for example, plastic. Zhang, on the other hand, is directed to thin film transistors formed on a glass substrate. The transistors in Zhang are formed from layers of very thin silicon film deposited on the glass substrate.

Purpose. Orcutt provides a structure that deals with the problem of differing coefficients of thermal expansion and provides a rigid member for solving that problem. Zhang provides for a thin amorphous silicon film for the purpose of shielding transistors

in a thin film transistor device from light transmitted from the substrate side of the TFT device.

All these differences point to that Orcutt and Zhang are in non-analogous arts. Furthermore, Appellants' invention deals with the solution to yet a third problem, namely, shielding an integrated circuit from light used for causing the switching of transistors during a light attack. A person seeking to protect an integrated circuit like the one in Orcutt would not be motivated to look to a disparate technology such as the thin film transistor device technology of Zhang.

In *KSR* quoted with approval the Federal Circuit's statement in in *In re Kahn that* "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn,* 441 F.3d 977, 988, 778 USPQ2d 1329, 1336 (Fed. Cir. 2006), *quoted* in *KSR*, 550 U.S. at ____, 82 USPQ 2d at 1396. In the Office Action, the Examiner offers "the ordinary artisan would have been motivated to modify Orcutt for at least the purpose of providing protection to certain portions of the chip from incident light of the specific wave lengths that the device is expected to be exposed to." Appellants disagree with this reasoning.

The *KSR* court identified a number of possible rationales to support a conclusion of obviousness. *KSR,* 82 USPQ2d 1385. It appears that the Examiner's proffered rationale most closely matches the "(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention." *MPEP 2143,*

8th ed. Rev. 6. There is absolutely no teaching or suggestion in Orcutt or Zhang to suggest that Orcutt is prone to attack by being exposed to infrared radiation. Infrared radiation is not "incident light … that [Orcutt's] device is expected to be exposed to.

There is no teaching, suggestion or motivation to combine Orcutt and Zhang. Orcutt teaches an "integrated circuit device [that] includes a rigid planar member of cover affixed to and overlaying at least a portion of the upper surface of a semiconductor integrated circuit bar. The upper surface of the planar member is textured to lock the member to the encapsulating medium, and has a thermal coefficient of expansion similar to that of the integrated circuit bar" (Orcutt, Abstract). As such, no external attack by means of electromagnetic radiation is envisioned, and no particular treatment of the "rigid planar member" for shielding against electromagnetic radiation is taught or suggested. Further, Zhang makes no mention of electromagnetic radiation in the infrared range and gives no teaching, suggestion or motivation to combine the application of a phosphorous doped silicon layer with any other structure to come up with the structure of Claim 1. Therefore, there is no teaching, suggestion or motivation to combine Orcutt and Zhang, and Claim 1 is not obvious over Orcutt in light of Zhang.

Only with the benefit of a hindsight analysis would a person attempting to solve the problem of exposure to IR radiation know to use a dopant concentration as set forth in Zhang. Appellants respectfully submit that there is no indication in Zhang that the dopant concentration set forth therein would be useful to block IR radiation. The Examiner relies on the Appellants' disclosure for that teaching. Office Action, Page 5, lines 2-3. Thus, a person looking to solve the problem would have to have the benefit of

Appellants' disclosure to know to look for a teaching that a concentration of dopant as suggested in Zhang could be used to block IR radiation and that therefore Zhang's dopant concentration (albeit from a very different field of endeavor) could be attempted for blocking IR radiation in light attacks against integrated circuits. Not only is that a classic case of hindsight analysis, here, the Examiner's argument implicitly admits to the hindsight analysis.

For the foregoing reasons, Claim 1 is not obvious over Orcutt in view of Zhang. Accordingly, Appellant respectfully requests reversal of the rejection.

Claim 20

Claim 20 as recites:

> A portable article … an additional layer of silicon that; is sealed to the active face of the silicon substrate layer by a sealing layer; and covers at least part of said active face; and comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm.

Thus, Claim 20 recites similar limitations as Claim 1, therefore, by virtue of the arguments presented in response to the rejection of Claim 1, Claim 20 is not obvious over Orcutt in light of Zhang.

Claim 26

Claim 26 recites:

> A chip for a chip-containing portable article comprising:
>
> a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and
>
> physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than

1 μm comprising silicon dopants in the face of the silicon substrate layer that is opposite to the active face.

The arguments set forth above in support of Claim 1 are incorporated herein. Claim 26 is patentable over Orcutt and Zhang at least for the reasons given there. Claim 26 further recites "physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising silicon dopants in the face of the silicon substrate layer that is opposite to the active face." Zhang recites a thin film of amorphous silicon to protect against incident light and a very thin film of silicon for forming the transistor layer. It would be inconceivable that such a teaching of thin layers could lead a person to modify a portion of another layer, i.e., the rigid planar layer of Orcutt by doping to thereby provide light shielding in the IR spectrum.

Claim 29

Claim 29 stands rejected over the combination of Orcutt, Zhang, and Kobachi.

Claim 29 recites:

A chip for a chip-containing portable article comprising:

a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising surface irregularities in the face of the silicon substrate layer that is opposite to the active face.

The arguments set forth above in support of Claim 1 are incorporated herein. Claim 29 is patentable over Orcutt and Zhang at least for the reasons given there. Claim

29 further recites "physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising surface irregularities in the face of the silicon substrate layer that is opposite to the active face."

As noted above, Zhang comes from an art that is non-analogous to Orcutt and a person of ordinary skill in the art of Orcutt (integrated circuit packaging) would not be motivated to turn to the art of Zhang (thin-film transistors for LCD displays) to find solutions. Similarly, Kobachi comes from an art that is also non-analogous to Orcutt and Zhang. While Orcutt is in the art of integrated circuit packaging and Zhang, in the art of thin-film transistors, Kobachi deals with the detection of objects by reflecting light of said objects. Appellants posit that Kobachi is also in such a vastly different art from Appellant, Orcutt, and Zhang, that no person would ever consider going to that reference to find solutions to the problems considered by Appellant (or Orcutt or Zhang).

Consider Figure 21 of Kobachi. A light source 210 emits light (arrows pointing upwards on Figure 21) that reflect from a reflective object 211 producing reflected light (arrows pointing downwards in Figure 21) radiating against light receiving elements 212a through 212d. By detecting light at 212a through 212d, it may be surmised that an object 211 has been present causing the reflection of light. It may further be possible to ascertain certain properties of object 211. To avoid being influenced by light from external sources, the assembly is shielded by an optical film structure 325. Now consider Figure 22 (the accompanying text (Kobachi, Col. 15, Lines 3-10) being cited by the Examiner (Office Action, Page 12, Lines 2-6, and Line 15)). In Figure 22, the external

light is diffused by irregular structures on the outer surface of the package 219. The irregular structures scatter the external light.

Appellants do not claim to have invented using an irregular structure to scatter light generally which is all that Kobachi can stand for. Appellants concede that it has been previously discovered that light rays that hit irregularly shaped structures scatter. What Appellants have invented, however, is the use of this property in designing a structure that shields circuits integrated into a silicon substrates from the action of electromagnetic radiation in the infrared range by providing surface irregularities on the face of the silicon substrates. Appellants posit that the fact that the Examiner had to go to such a distant art to find a reference for such a well-known concept and apparently was unable to find a similar reference in a more near-lying art is in of itself evidence of the unobviousness of creating the structure that Appellants have invented and claimed. Only through hindsight, by considering Appellants' disclosure, would a person be moved to think of scattering external light radiated against the structure of Orcutt for the purpose of shielding the circuits thereon from light-based attacks by designing in surface irregularities into the silicon substrate.

For these reasons Claim 29 is patentable over Orcutt and Zhang, in combination with Kobachi.

Claim 30

Claim 30 recites:

> A chip for a chip-containing portable article comprising:
>
> a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising deposition of metal on the face of the silicon substrate layer that is opposite to the active face.

The arguments set forth above in support of Claim 1 are incorporated herein. Claim 30 is patentable over Orcutt and Zhang at least for the reasons given there. Claim 30 further recites "physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising deposition of metal on the face of the silicon substrate layer that is opposite to the active face." While Zhang teaches a metal layer as an alternative shielding in the context of protecting TFT transistors from visible light, there is no teaching or suggestion therein to use such a layer to protect against IR radiation. Thus, the arguments given above in support of Claim 1 are equally applicable to Claim 30, for example, that one would not be motivated to look to the TFT technology solutions of Zhang for solutions to the problem of dealing with exposure to IR radiation in integrated circuit devices. Furthermore, there is no indication that Orcutt would benefit from shielding from IR light. For these reasons Claim 30 is patentable over Orcutt and Zhang.

Claims 5-7, 10, 12-17, 19, 21-25

The dependent Claims 5-7, 10, 12-17, 19, 21-25 each depend from Claim 1, Claims 27-28 depend from Claim 26, Claims 31 and 32 depend from Claim 30. These claims inherit the limitations of their respective base claims, provide further unique and non-obvious combinations, and are patentable over Orcutt and Zhang for the reasons given in support of the independent claism and by virtue of such further combinations.

Claims 10, 12 and 13

Claims 10, 12, and 13 were rejected under 35 USC 103(a) as unpatentable over Orcutt in view of Zhang and in further view of Kobachi. As argued hereinabove Claim 1, from which Claims 10, 12, and 13 depend are patentable over Orcutt and Zhang. Kobachi also fails to teach or suggest "an additional layer of silicon that: is sealed to the active face of the silicon substrate layer by a sealing layer; covers at least part of said active face; and comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm." Therefore, Claim 1 is patentable over the combination of Orcutt, Zhang and Kobachi. Claim 10, 12, and 13 all depend ultimately from Claim 1 and inherit all the limitations thereof. Therefore, Claim 10 is patentable over the combination of Orcutt, Zhang, and Kobachi for the reasons given in support of Claim 1.

Conclusion of Argument

Appellants have argued hereinabove that the rejections under 35 USC 103(a) are improper and that the claims are patentable over the prior art. Accordingly, Appellants respectfully request reversal of the rejections of Claims 1,5-7, 10, 12-17 and 19-32 and their early allowance.

Respectfully Submitted,

/Pehr Jansson/

Pehr Jansson
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8. Claims appendix

Listing of the claims:

1. A chip for a chip-containing portable article comprising:

   a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

   an additional layer of silicon that:

   is sealed to the active face of the silicon substrate layer by a sealing layer;

   covers at least part of said active face; and

   comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm.

2. (Withdrawn)

3. (Withdrawn)

4. (Cancelled)

5. A chip according to Claim 1, wherein the physical means for providing physical protection against the action of electromagnetic radiation are silicon dopants.

6. A chip according to Claim 5, wherein the concentration of silicon dopants lies in the range 10^{17} to 10^{20} atoms per cm^3.

7. A chip according to Claim 5, wherein the silicon dopants are phosphorus or boron.

8. (Cancelled)

9. (Cancelled)

10. A chip according to Claim 1, wherein the physical means for providing physical protection against the action of electromagnetic radiation are formed by surface irregularities.

11. (Cancelled)

12. A chip according to claim 10, wherein the surfaces irregularities are provided in the face of the additional layer of silicon that is in contact with the sealing layer.

13. A chip according to Claim 10, wherein the surface irregularities are provided in the face of the additional layer of silicon that is opposite to the face that is in contact with the sealing layer.

14. A chip according to Claim 1, wherein the physical means for providing physical protection against the action of electromagnetic radiation are formed by at least one deposition of metal on the additional layer of silicon.

15. A chip according to Claim 14, wherein the metal deposition has a thickness greater than 50 Å.

16. A chip according to Claim 14, wherein the metal deposition is on the face of the additional of silicon that is in contact with the sealing layer.

17. A chip according to Claim 14, wherein the metal deposition is on the face of the additional layer of silicon that is opposite to the face that is in contact with the sealing layer.

18. (Cancelled)

19. A chip according to claim 16, wherein the metal deposition has a thickness of about 100 Å.

20. A portable article provided with a chip comprising:

a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

an additional layer of silicon that:

is sealed to the active face of the silicon substrate layer by a sealing layer;

covers at least part of said active face; and

comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm.

21. The chip according to Claim 5 wherein the silicon substrate layer comprises:

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm; and

wherein said physical means of the silicon substrate layer comprises silicon dopants in the face of the silicon substrate layer that is opposite to the active face.

22. The chip according to Claim 21, wherein the concentration of silicon dopants in the silicon substrate layer lies in the range 10^{17} to 10^{20} atoms per cm^3.

23. The chip according to Claim 22, wherein the silicon dopants in the silicon substrate layer are phosphorus or boron.

24. A chip according to Claim 10 wherein the silicon substrate layer comprises:

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm: and

wherein said physical means comprises surface irregularities in the face of the silicon substrate layer that is opposite to the active face.

25. A chip according to Claim 14 wherein the silicon substrate layer comprises:

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm; and

wherein said physical means comprising deposition of metal on the face of the silicon substrate layer that is opposite to the active face.

26. A chip for a chip-containing portable article comprising:

a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising silicon dopants in the face of the silicon substrate layer that is opposite to the active face.

27. A chip according to Claim 26, wherein the concentration of silicon dopants lies in the range 10^{17} to 10^{20} atoms per cm^3.

28. A chip according to Claim 27, wherein the silicon dopants are phosphorus or boron.

29. A chip for a chip-containing portable article comprising:

a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising surface irregularities in the face of the silicon substrate layer that is opposite to the active face.

30. A chip for a chip-containing portable article comprising:

a silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and

physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm comprising deposition of metal on the face of the silicon substrate layer that is opposite to the active face.

31. A chip according to Claim 30, wherein the metal deposition has a thickness greater than 50 Å.

32. A chip according to claim 30, wherein the metal deposition has a thickness of about 100 Å.

9. Evidence appendix

1. Intel Museum – Microprocessor Hall of Fame, http://www.intel.com/museum/online/hist%5Fmicro/hof/, retrieved and printed on May 20, 2009)
2. Intel 80386/80387 Memorabilia, CPU World, http://www.cpu-world.com/Memorabilia/80386/, retrieved and printed on May 20, 2009).

10. Related proceedings appendix

Not applicable.